(12) UK Patent Application (19) GB (11) 2 332 564 (13) A

(43) Date of A Publication 23.06.1999

(21) Application No 9824541.8

(22) Date of Filing 09.11.1998

(30) Priority Data
(31) 692811997 (32) 16.12.1997 (33) KR

(51) INT CL[6]
H01L 21/324 21/335 33/00

(52) UK CL (Edition Q)
H1K KHAC KLHX K1EA K1FX K3F K3P2C K3P2D K3P2Y K3P5 K9C9 K9N3 K9R1

(56) Documents Cited
US 5559343 A
Journal of Crystal Growth, vol 192, no 3-4, pp 395-401
Japanese Journal of Applied Physics, Part 2 (Letters), vol 3 7, no 2A, pp L161-L163

(58) Field of Search
UK CL (Edition Q) H1K KEAX KELX KFX KHAC KKAX KKB KLHA KLHX KLX KMWP KMWX
INT CL[6] H01L , H01S
online: EPODOC,WPI,JAPIO,INSPEC

(71) Applicant(s)
LG Semicon Co Ltd
(Incorporated in the Republic of Korea)
1, Hyangjeong-dong, Heungduk-gu, Cheongju-si, Chungcheongbuk-do, Republic of Korea

(72) Inventor(s)
Ki Bum Kim
Tae Sik Yoon
Jang-Yeon Kwon

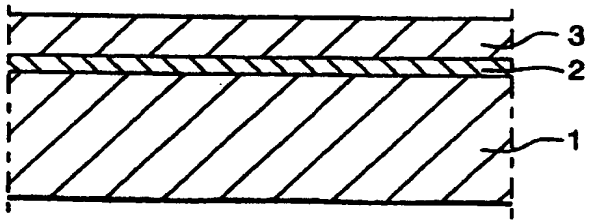
(74) Agent and/or Address for Service
Withers & Rogers
Goldings House, 2 Hays Lane, LONDON, SE1 2HW, United Kingdom

(54) Abstract Title

Method of forming quantum dots in a semiconductor device

(57) A method of forming quantum dots using agglomeration of a conductive layer, includes the steps of forming a first insulating layer 1 on a substrate, forming a conductive layer 2 on the first insulating layer, forming a second insulating layer 3 on the conductive layer, and annealing the conductive layer between the first and second insulating layers to agglomerate the conductive layer. Alternatively, the second insulating layer may be dispensed with. Methods are described using insulating layers of Sio_2 and a conductive layer of $Si_{0.7}Ge_{0.3}$. Annealing may be conducted in a vacuum or in an atmosphere of nitrogen.

FIG. 3



GB 2 332 564 A

FIG. 1

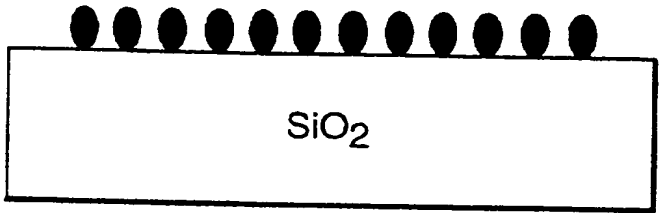


FIG. 2

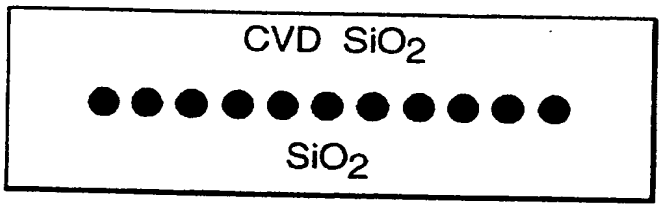


FIG. 3

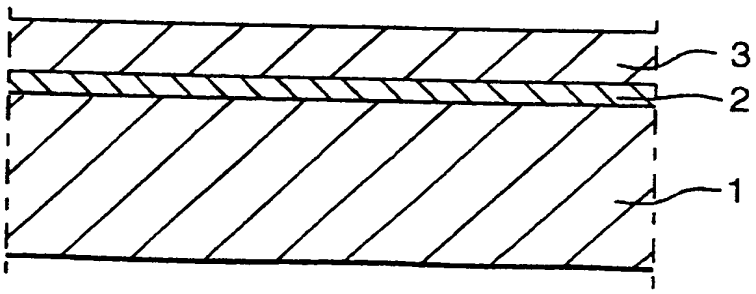


FIG. 6A

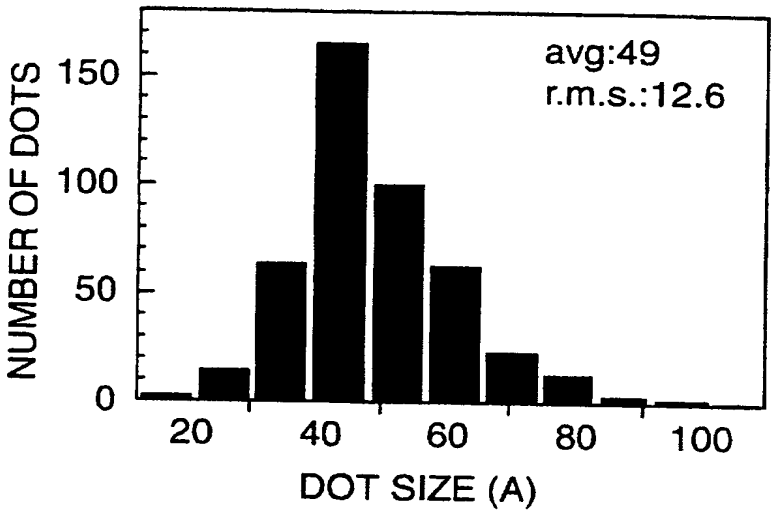


FIG. 6B

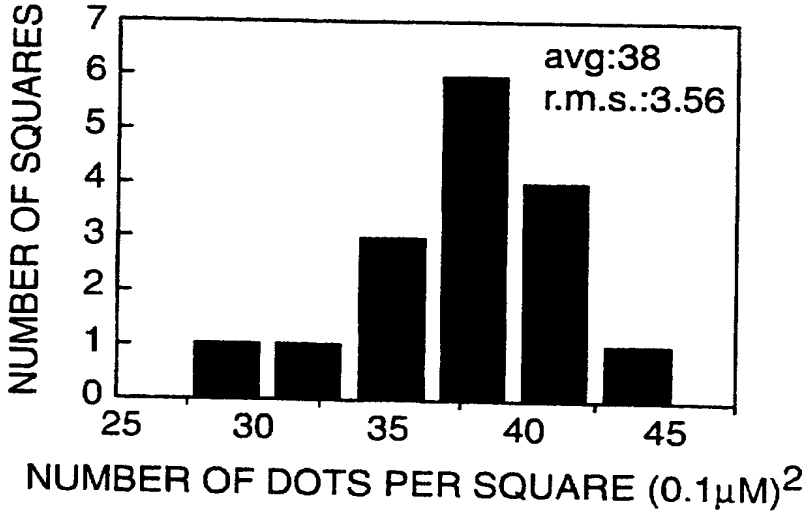


FIG. 5

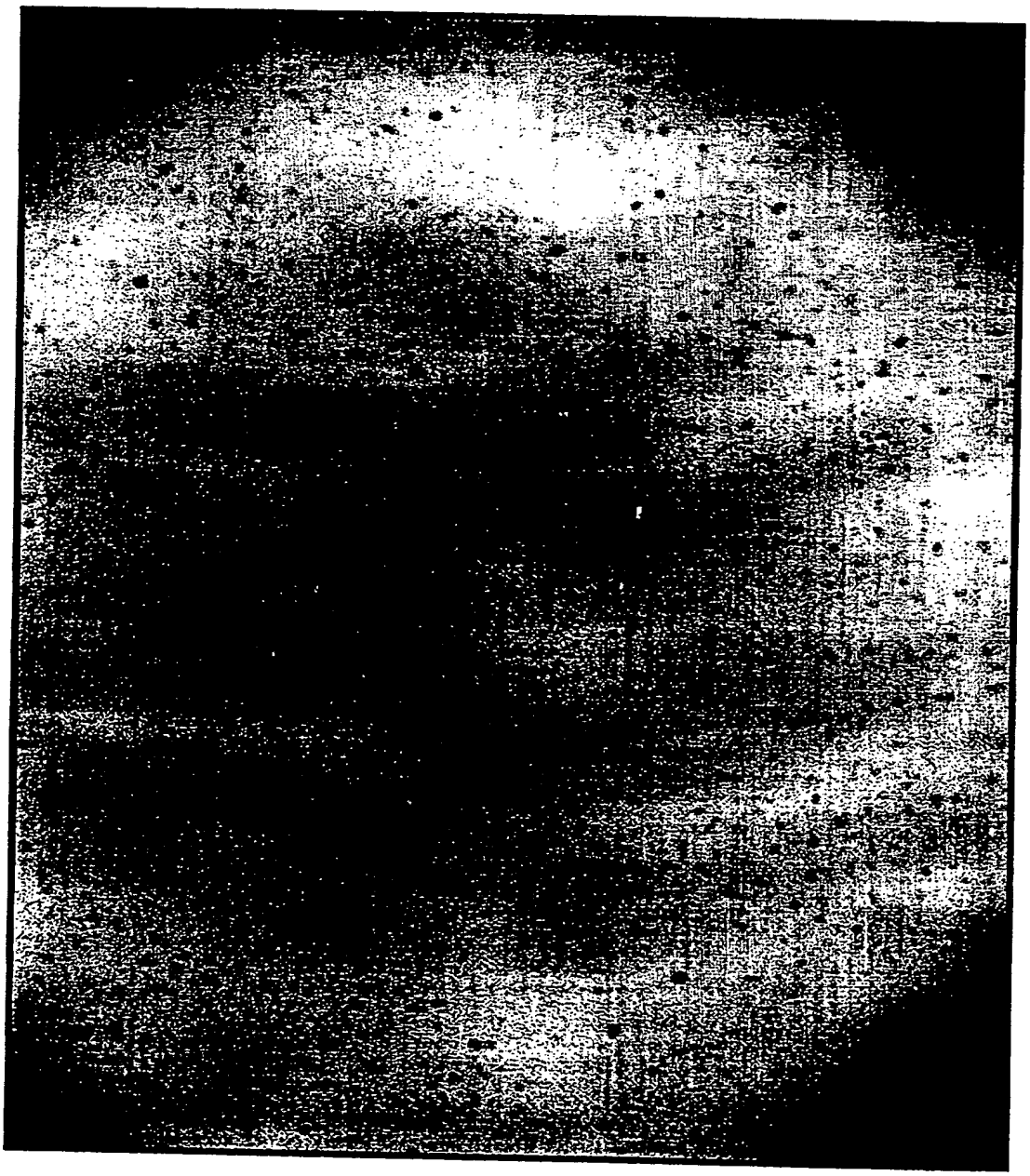


FIG. 4(a)

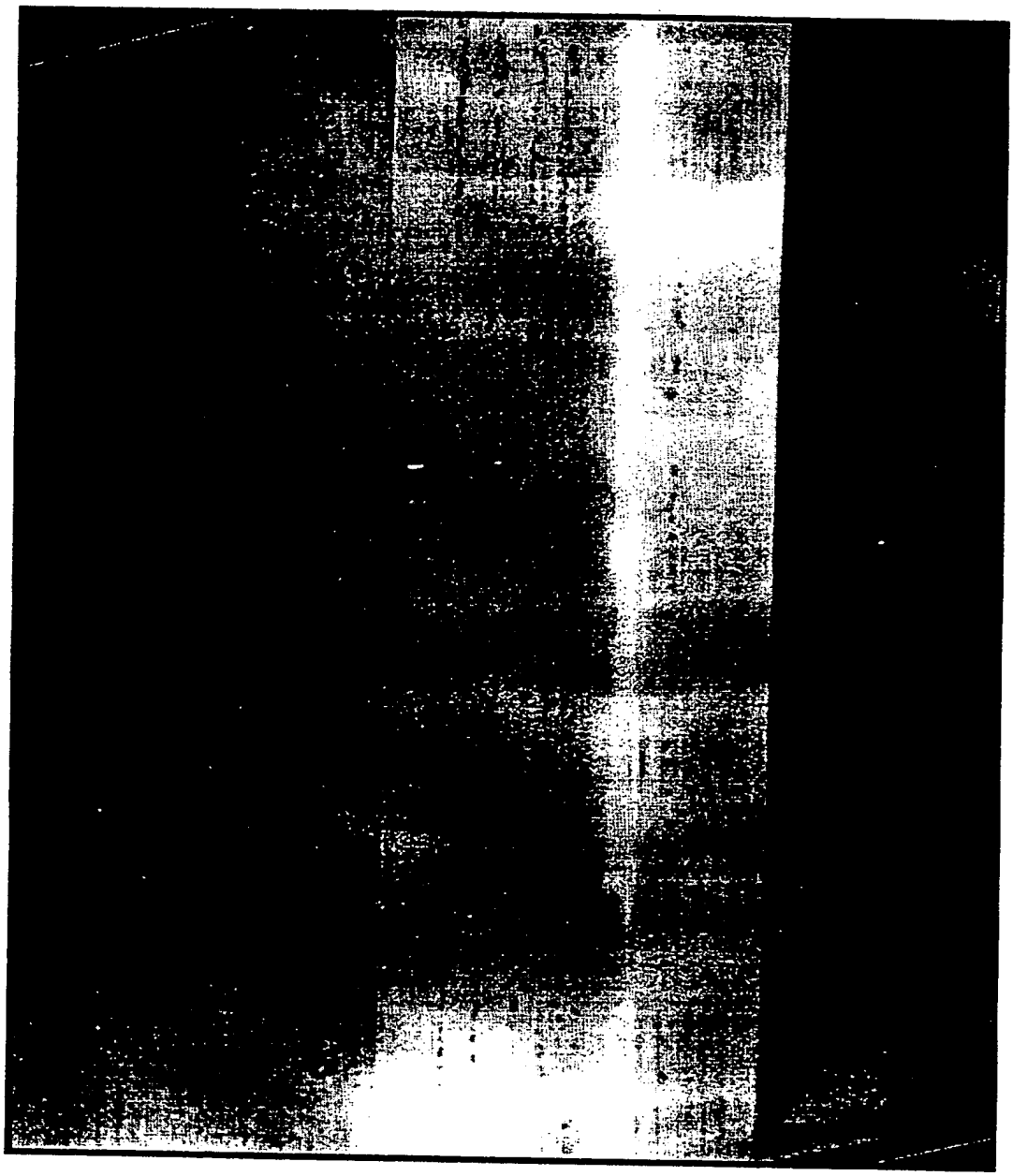


FIG. 4(b)

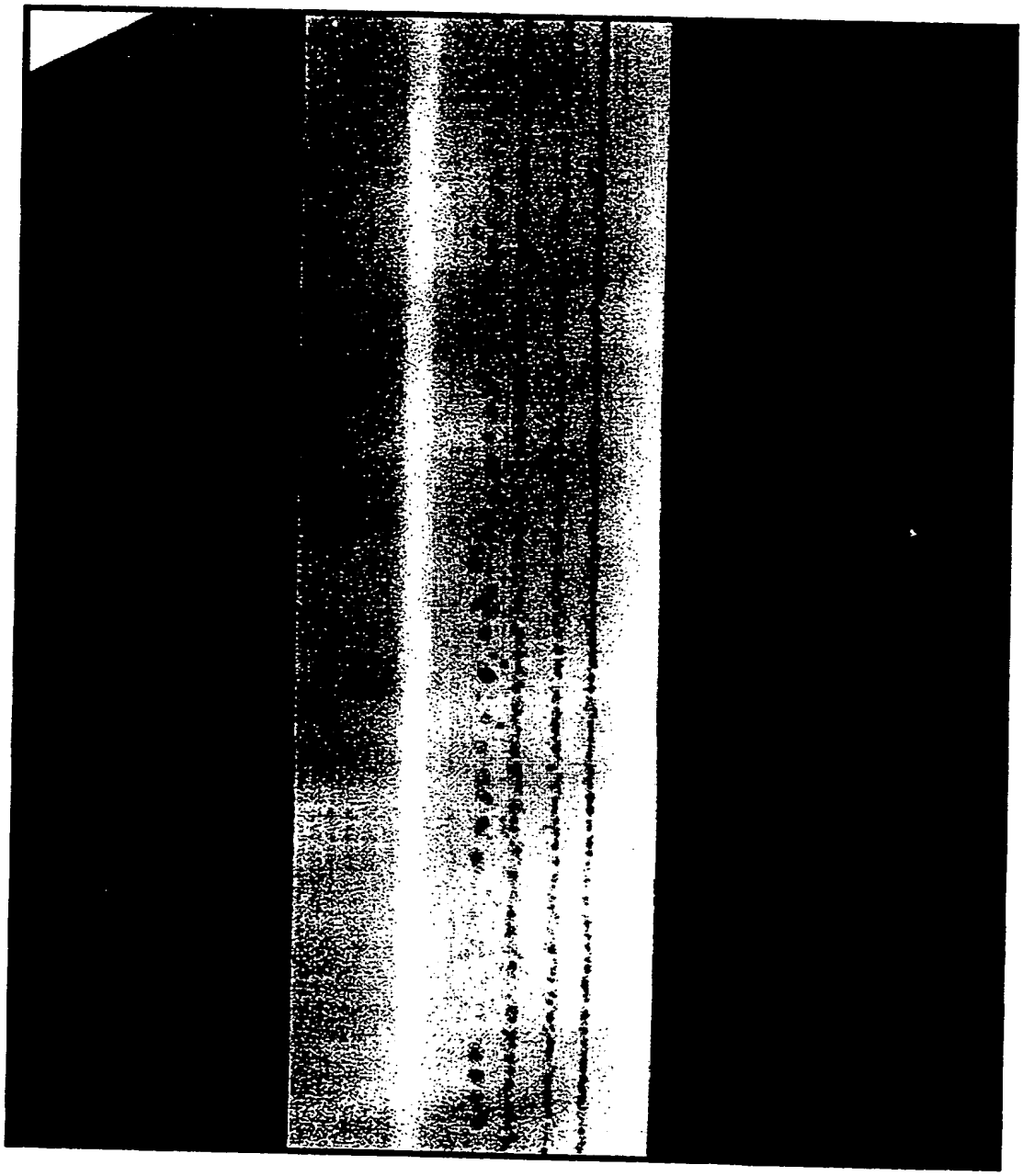


FIG. 7

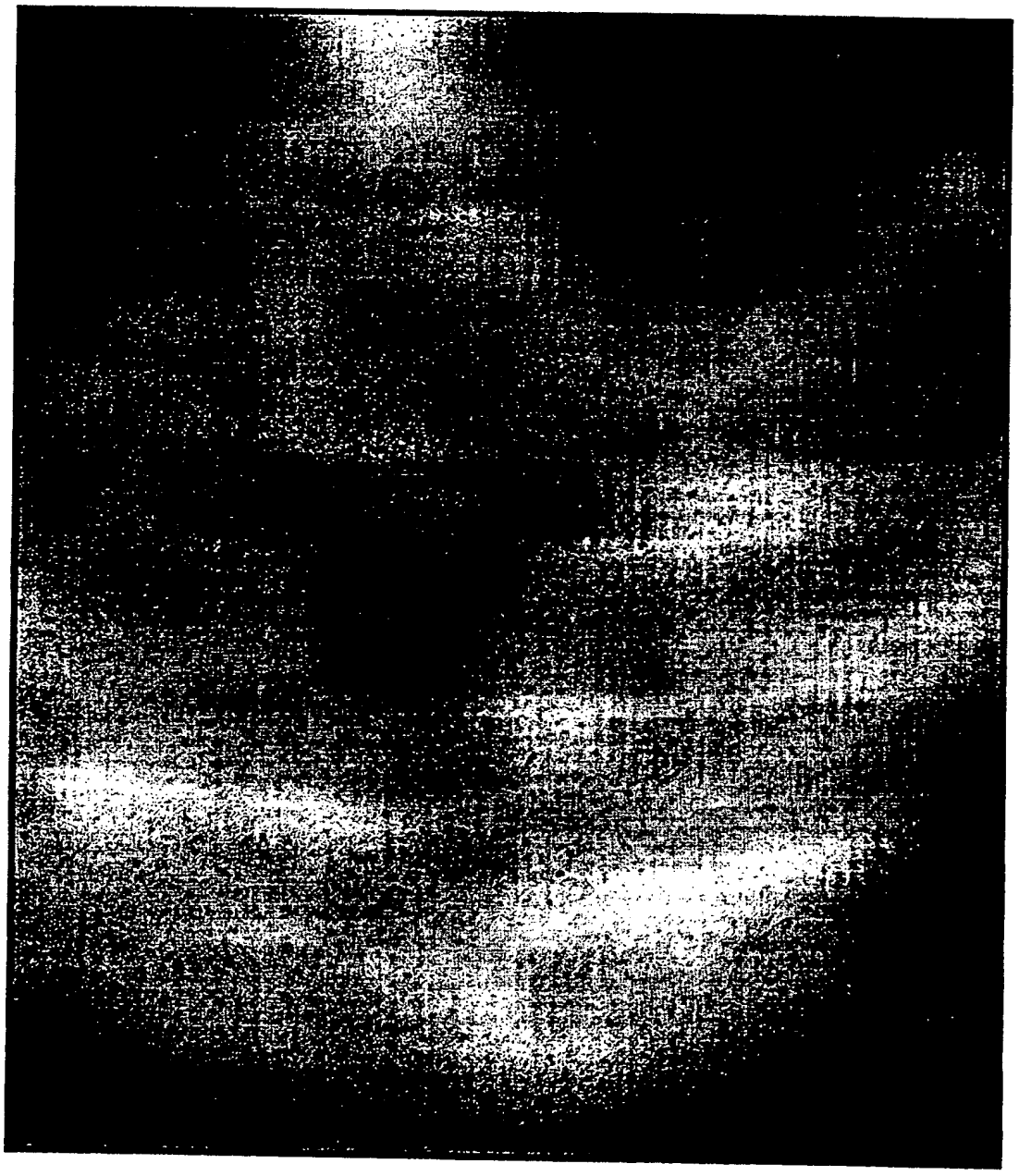


FIG. 8

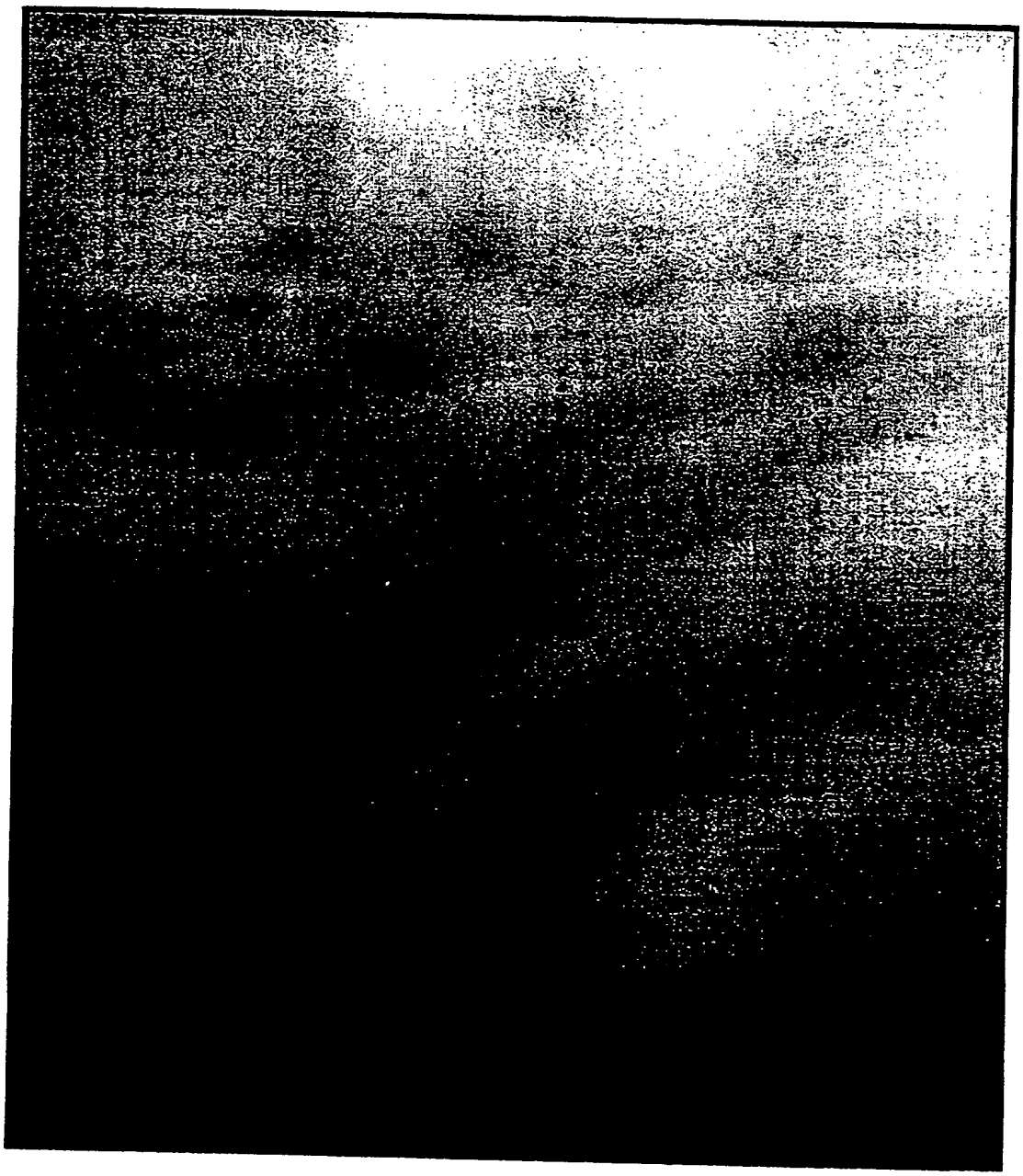


FIG. 9A

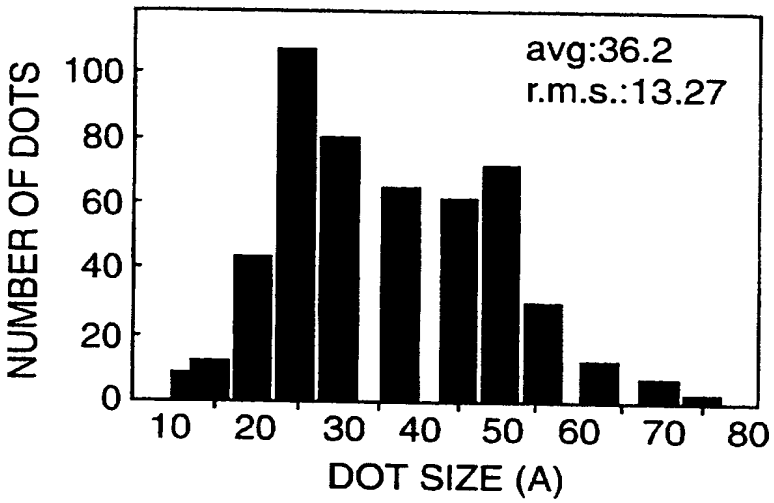
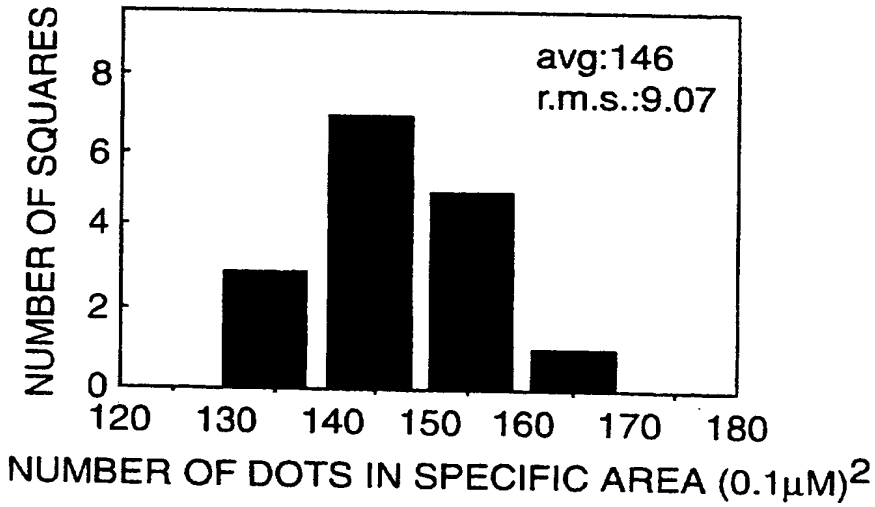


FIG. 9B



METHOD OF FORMING QUANTUM DOTS IN A SEMICONDUCTOR DEVICE

The present invention relates to a method of forming quantum dots in a semiconductor device.

In view of a forseen limitation to the MOS structure, which is a basic structure of a semiconductor memory device, a new semiconductor fabrication technology needs to be developed for increasing integration of semiconductor memory devices. In the case when the semiconductor memory device is of the MOS structure, it is assumed that the switching by means of the gate voltage that has been used as an operating principle of an MOS cell until now, is no longer possible for a semiconductor memory device with a device packing density of 4 giga DRAM range because the distance between the source and the drain becomes as small as about 0.13μm (S. Wolf, "Silicon Processing; for the VLSI Era", V2, chap.8). In other words, it is foreseen that the limitation of integration of the MOS structure is about 4 giga DRAM because, if the separation of the source and drain becomes reduced, malfunctions of the device may occur due to tunnelling between the source and the drain and through an oxide film formed on the gate even in the absence of gate voltage . Therefore, in order to fabricate a device of giga or tera class, a form of device other than the current MOS structure needs to be employed, and such a device is the SET(Single Electron Transistor)[see K. K. Likharev, IBM J. Res. Develop. 32(1) p144(1988)] currently suggested by many research groups.

The following problems need to be resolved for fabrication of the SET for use as a switching device of a DRAM. First, from the point of view of the physical performance of the SET, the size of the quantum dot required

for an SET cell should be less than 10nm so that operation of the cell does not show any error due to thermal vibration. Therefore, a quantum dot size of at least a few nanometers is required to allow operation of the SET at room temperature. As well as the above SET cell operation requirement in view of physical performance of the SET, it is also necessary to take into account that development of a process for forming quantum dots is required which allows integration on a wafer of a size greater than 20 to 30 cms (8 to 12 inches).

When the results of research up to now is reviewed, it can be seen that the development is still at a stage at which the operating principle of the SET device is established. In other words, the development is still at a stage at which EBL (Electron Beam Lithography) and RIE (Reactive Ion Etching) is mostly used to form quantum dots. [K. Nakazato, T. J. Thornton, J. White, and H.Ahmed, Appl. Phys. Lett. 61(26), 3145(1992)], [D. J. Paul, J.R. A. Cleaver, H. Ahmed, and T. E. Whall, Appl. Phys. Lett. 63(5), 631(1993)], [D. Ali and H. Ahmed, Appl. Phys. Lett. 64(16) 2119(1994)], [E. Leobandung, L. Guo, Y, Wang, and S. Y. Chou, Appl. Phys. Lett. 67(7), 938(1995)], [K. Nakazato, R. J. Blankie, and H. Ahmed, J. Appl. Phys. 75(10), 5123(1992)], [Y. Takahashi, M. Nagase, H. Namatus, K. Kurihara, K. Iwadate, Y. Nakajima, S.Horiguchi, K. Murase, and M. Tabe, IEDM 1994, p 936], and [E. Leobandung, L. Guo, and S. Y. Chou, IEDM 1995, p365].

Such a quantum dot has application in a memory device of an SET and in a light emitting device. The application in a light emitting device is made possible on the principle that an energy band gap becomes greater as a dimension of the material becomes smaller, with a subsequent decrease of the wave length of the emitted light. That is, if a material

becomes reduced to a nano-scale, the material emits light of a wave length different from the wave length of the same material in bulk. Utilizing the dependence of the wave length of an emitted light on the size of the material, the size of quantum dot can be controlled to obtain light of a desired wave length. Such research is actively underway in III-V semiconductor fields, which are typical light emitting materials. [D. Leonard, M. Krishnamurthy, C. M. Reaves, and S. P. Denbaars, and P. M. Petroff, Appl. Phys. Lett. 63(23), 3203(1993)] and [O.I. Micic, J. Sprague, Z. Lu, and A. J. Nozik, Appl. Phys. Lett. 68(22), 3150(1996)]. There are reports that silicon Si or germanium Ge, which has an indirect gap, also emit blue light when their size is reduced. By forming a quantum dot of such a silicon or germanium, application in a light emitting device is also possible. [Y. Kanemitsu, H. Uto, and Y. Masumoto, Appl. Phys. Lett. 61(18), 2187(1992)] and [H. Morisaki, H. Hashimoto, F. W. Ping, H. Nozawa, and H. Ono, J. Appl. Phys. 74(4), 2977(1993)].

In the case when nano-scale quantum dots are used in an SET, the way in which the quantum dots should be distributed within a cell is basically dependent on the form of the SET structure to be used. SET structures suggested to date may be divided into two forms. One form of SET structure has, like the MOS structure, a source, a drain and a gate, together with a channel with the quantum dots which allow discrete flow of electrons; a channel with an insulator and an array of multi-channel conductors(quantum dots), allowing discrete tunneling of electrons through the quantum dots, i.e., the channel has a form in which the quantum dots are embedded in the insulator [K. Nakazato, T. J. Thornton, J. White, and H. Ahmed, Appl. Phys. Lett. 61(26), 3145(1992)], [D. J. Paul, J. R. A.

Cleaver, H. Ahmed, and T.E. Whall, Appl. Phys. Lett. 63(5), 631(1993)], [D. Mi and H. Ahmed, Appl. Phys. Lett. 67(7),938(1995)], [K. Nakazato, R. J. Blankie, and H. Ahmed, J. Appl. Phys. 75(10), 5123(1992)], [Y.Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K.Murase, and M. Tabe, IEDM 1994, p 938], [E. Leobandung, L. Guo, and S. Y. Chou, IEDM 1995, p365], [O. I. Micic, H. Sprague, Z. Lu, and A. J. Nozik, Appl. Phys. Lett. 68(22),3150(1996)] and [D. V. Averin and K. K. Likaharev, in "Single Charging Tunneling", edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992) p311]. This represents the simplest structure required for transferring electrons by discrete tunnelling. Though there is research which verifies that the Coulomb blockade effect required for operating an SET cell is also achieved even though the channel is formed with a two dimensional continuous conductive line through which electrons transfer[M. A. Kastner, Rev. Mod. Phys. 64(3), 849(1992)] and [R. A. Smith and H. Ahmed, J. Appl. Phys. 81(6), 2699(1997)], the surest way of inducing the discrete tunnelling of electrons is by providing quantum dots in an insulator.

The other form of SET structure also has a structure similar to the MOS structure, with a floating point for charging electrons in the channel thereof for reducing current flowing through the channel[S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. 68(10), 1377(1994)], [K. Yano, T, Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE Trans. Electron Devices 41(9), 1628(1994)], and [A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, Appl. Phys. Lett. 70(13),1742(1997)]. This form of SET structure is similar to

an EPROM (Electrically Programmable Read Only Memory) which utilizes a hot carrier effect in reverse. Such a reduction of current shows a quantized change by electron charging when a Coulomb blockade effect appears at which electrons charged in the quantum dots prevent successive charging of further electrons. For this, the charging energy of the cell should be lower than the thermal energy of the cell, and the voltage drop caused by the charging should be large enough to be sensed in order to be used as a memory cell, for which the quantum dot size should be in the range of a few nano-meters.

Firstly, the memory function of the device is operative only at a super low temperature, because the quantum dots in the device have a limitation on their sizes due to the technological limitation of EBL and RIE. Moreover, it is apparent that the formation of the quantum dots by EBL and RIE used up to now mostly is not appropriate for obtaining adequate through-put as well as for integrating on a large sized wafer. Therefore, development of a quantum dot forming process which can be integrated on a large sized wafer and which can provide an adequate through-put, other than using an EBL and RIE process, is desirable for utilizing an SET as the next generation integrated circuit.

Secondly, in the case when the quantum dots are used as a light emitting device, the size of the quantum dot needs to be controlled to obtain light of a desired wave length, all of which conditions require a size of the quantum dot in a range of a few nano-meters, that has heretofore not been developed.

Accordingly, the present invention is directed to a method of forming quantum dots in a semiconductor device that substantially obviates, or at least reduces one or more of the

problems due to limitations and disadvantages of the art discussed above.

An object of the present invention is to provide a method of forming quantum dots in a semiconductor device, in which uniform quantum dots of a few nano-meter size can be formed for application as an SET cell as well as an optical application such as a light emitting cell.

In accordance with one aspect of the present invention, there is provided a method of forming quantum dots in a semiconductor device, comprising the steps of forming an insulating layer on a substrate, forming a conductive layer on the insulating layer, and annealing the conductive layer on the insulating layer to agglomerate the conductive layer.

In other aspect of the present invention, there is provided a method of forming quantum dots in a semiconductor device, comprising the steps of, forming a first insulating layer on a substrate, forming a conductive layer on the first insulating layer, forming a second insulating layer on the conductive layer, and annealing the conductive layer between the first and second insulating layers to agglomerate the conductive layer.

Embodiments of the method of forming quantum dots, each in accordance with the present invention, will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a schematic diagram illustrating a method of forming quantum dots by means of a free surface agglomeration;

Fig. 2 is a schematic diagram illustrating a method of forming quantum dots by means of an interface agglomeration ;

Fig. 3 is a section of part of a device formed bya first preferred method;

Figs. 4(a) and (b) are cross-sectional TEM micrographs of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed in an N_2 atmosphere for 10 min. at 800 °C and 900 °C respectively;

Fig. 5 is a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed in an N_2 atmosphere for 10 min. at 800 °C,

Fig. 6a illustrates a quantum dot size distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800 °C for 10 min. in an N_2 atmosphere;

Fig. 6b illustrates a spatial quantum dot distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800 °C for 10 min. in an N_2 atmosphere;

Fig. 7 is a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed at 800 °C for 10 min. in vacuum(pressure < 10^{-6} torr);

Fig. 8 is a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed at 800 °C for 1 hour in vacuum(pressure < 10^{-6} torr);

Fig. 9a illustrates a quantum dot size distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800°C for 10 min. in vacuum; and

Fig. 9b illustrates a spatial quantum dot distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800 °C for 10 min. in vacuum.

In the methods of forming quantum dots in accordance with the present invention, there are primarily a method of forming quantum dots by means of agglomeration of a conductive layer and a method of forming quantum dots by means of simultaneous agglomeration and selective oxidation of a conductive layer. In the method of forming quantum dots by means of agglomeration of a conductive layer, there are cases where the agglomerated conductive layer exists on a free surface, as shown in Figure 1, and cases where the agglomerated

conductive layer exists at an interface, as shown in Figure 2.

The method of forming quantum dots by means of free surface agglomeration starts with a step of forming an insulating layer on a substrate, preferably as an insulating film, such as a silicon oxide(SiO_2) film, into which oxygen or water vapour can be diffused. A conductive layer is formed on the insulating layer and subjected to annealing, to agglomerate the conductive layer . The conductive layer may be formed of an alloy(Si_{1-x}-$metal_x$) of Si and a material selected from Si, Ge, $Si_{1-x}Ge_x$, Al, Au, Cu, Pt, Cr, Ru and Ta, or an alloy(Ge_{1-x}-$metal_x$)of Ge and the aforementioned material, or an alloy of the aforementioned materials, where $0<x<1$. In order to prepare a test specimen, the insulating layer is formed of a silicon oxide film SiO_2, and copper Cu is deposited thereon to a thickness of around 5.0×10^{-7} cm (50 Å) as the conductive layer and subjected to annealing at 800 °C in a nitrogen atmosphere, resulting in the formation of quantum dots of about 5.0×10^{-6} cm(500 Å) size. This result may be interpreted as the quantum dots being formed of a size about 10 times greater than the thickness of the deposited film due to the easy surface diffusion of the atoms. The quantum dots formed thus cannot be used as an SET because their size is too large. In this regard, the interface agglomeration can be expected to provide small sized quantum dots, because movements of the atoms in the conductive layer are restricted by the insulating layer, such as an SiO_2 layer, formed on the conductive layer and will not be easy to achieve. Size, and spatial distributions of the quantum dots are expected to be substantially uniform because the agglomerated layer is confined by the insulating layers at its upper and lower sides. The SET is based on the utilization of the quantum

mechanics involved in changing electrons into quantum dots by an external electric field, and the nano-scale transfer of electrons is dependent on the discrete energy levels. That is, the transfer of electrons is dependent on the dimensions of the device , such as sizes of the quantum dots with which the channel or capacitor of the device is formed as well as the intrinsic energy levels of the material. In other words, in order to induce the discrete tunnelling of electrons only by an external electric field without being influenced by room temperature thermal vibration, the electron charging energy should be greater than the thermal energy, for which entire capacitors in a capacitor array should have a value of a few μF. The device dimension should be nano-scale for satisfying such a condition. Moreover, as disctinct from a micro-dimension, when the dimension comes down to nano-scale, phenomena of quantum mechanics appear, of which one example is the resonant tunnelling. The resonant tunnelling, which is a tunnelling dependent on energy levels, is a phenomenon that appears when a material approaches nano-scale, at which discrete energy levels are involved wherein electron tunnelling occurs only when the energy level of an electron involved in tunnelling is not in a forbidden gap. Since the flow of electrons when a device dimension comes down to nano-scale is subject to quantum mechanics, the electrical performance of the device is dependent on the material and on the size of the quantum dots.

An explanation as to the difference arising in view of an agglomeration process as the quantum dot material is actually changed will be given below. Agglomeration is produced by movements of atoms driven by a force leading to the lowering of the total energy of the system in which the

atoms exist. As factors that determine such atomic movements, there are the magnitude of the driving force from the thermodynamic point of view and the mobility of the atoms from the kinetic point of view. Therefore, it can be foreseen that the size and distribution of the quantum dots may be different depending on the material of the agglomerated layer even if the agglomeration is conducted under the same conditions.

Fig. 3 illustrates a section of a device useful in illustrating a method for forming quantum dots in the case when the conductive layer exists at an interface .

Referring to Fig. 3, a first insulating layer 1 is formed on a substrate (not shown), the layer 1 preferably being, for example, of a silicon oxide SiO_2 into which oxygen or water vapour can be diffused. A conductive layer 2 is formed on the first insulating layer 1, and a second insulating layer 3 is formed on the conductive layer 2. The second insulating layer 3 is formed of a material identical to the material of the first insulating layer 1. Different conductive layers may be used for the material of the conductive layer 2 for the interface agglomeration, for example, different metals having large interfacial energy to the insulating layer of SiO_2. Metallic material and semiconductor material for the quantum dots in the SET may provide no difference in the Coulomb blockade effect, but may provide a difference in tunnelling probabilities. Also, it can be expected that there is a difference in electrical performance depending on the material of the quantum dots. Since the interface agglomeration is dependent on the interfacial energy and the speed of the atoms, there will be a difference of the interface agglomerations depending on the material of the quantum dots. As materials which have excellent interfacial stability to

silicon oxide film of the first insulating layer 1 and the second insulating layer 3 and can retard oxidation at an interface, the conductive layer 2 may be formed of an alloy(Si_{1-x}-$metal_x$) of Si and a material selected from Si, Ge, $Si_{1-x}Ge_x$, Al, Au, Cu, Pt, Cr, Ru and Ta, or an alloy(Ge_{1-x}-$metal_x$) of Ge and the aforementioned material, or an alloy($metal_{1-x}$-$metal_x$) of the aforementioned materials, where $0<x<1$. The conductive layer 2 between the first and second insulating layers 1 and 2 is then annealed, to agglomerate the conductive layer 2 into quantum dots.

An experimental result of the method will now be described with respect to quantum dots formed with the first and second insulating layers 1 and 3 of silicon oxide SiO_2 and the conductive layer 2 of $Si_{0.7}Ge_{0.3}$ by means of the interface agglomeration. As explained, whereas it can be expected that the interface agglomeration is dependent on the material of the agglomerated layer, at first, for the fabrication of an Si-based device, the conductive layer is formed of $Si_{0.7}Ge_{0.3}$, which is silicon added with 30 % of silicon in the $Si_{1-x}Ge_x$ alloy system for the purpose of improving atomic mobility, utilizing the selective oxidation effect of germanium in the annealing and changing quantum mechanic performance of the quantum dots. The experiments should be conducted while varying the germanium composition, for verifying changes both in the quantum dot formation and in electrical performance, such as resonant tunnelling, as the germanium added. The experimental result based only on 30 % of germanium will now be explained . SiO_2(first insulating layer 1) is deposited on a single silicon substrate to a thickness of 4.7×10^{-6}cm (470 Å) at 425 °C by LPCVD, and a conductive layer 2 of $Si_{0.7}Ge_{0.3}$ is deposited thereon to a thickness of 3.0×10^{-7}cm (30 Å) at 375°C.

Then, a CVD-SiO_2 layer (second insulating layer 3) is deposited thereon to a thickness of $1.3x10^{-6}$cm (130 Å) at 375 °C. In this instance, a similar experimental result can be obtained even if the SiO_2 is deposited to a thickness of $4.4x10^{-6}$ to $5.5x10^{-6}$cm (440~550 Å) at 400~550 °C by LPCVD, the conductive layer 2 of $Si_{0.7}Ge_{0.3}$ is deposited thereon to a thickness of $3.0x10^{-7}$ to $5.0x10^{-7}$cm (20~50 Å) at 300~450 °C, and the CVD-SiO_2 layer is deposited thereon to a thickness of $1.0x10^{-6}$ to $1.5x10^{-6}$ cm (100~150 Å) at 300 ~450 °C.

It can be expected that the formation of the quantum dots by means of the $Si_{0.7}Ge_{0.3}$ layer agglomeration may differ according to condition of the annealing, because, being a process for providing energy required for settling down the entire system energy to a lower state, the annealing determines an entire system energy equilibrium and the speed of the atoms. The temperature, atmosphere, and the time period are relevant annealing parameters, of which the annealing time period will not be critical if the time period required for the agglomeration is very short. This is sobecause once the driving force for the agglomeration is fixed by the annealing temperature and the quantum dots are formed by the agglomeration, there will not be any variation in the size and distribution of the quantum dots coming from inter-quantum point movement of the atoms. However, if the annealing is conducted, not in a vacuum, but in the atmospheric pressure of a tube furnace with residual oxygen and water vapour, the annealing time period can be an important parameter because the influence of the residual oxygen and water vapour present in the furnace is dependent on the time period of annealing. The experimental conditions relating to the above parameters are as follows:

TABLE 1

layer structure	SiO_2(130 Å)/$Si_{0.7}Ge_{0.3}$(30 Å)/SiO_2(470 Å)
annealing temperature	800 °C, 900 °C
annealing time	10 min, 1 hour
annealing atmosphere	N_2, vacuum(pressure < 10^{-6} torr)

Of the above annealing conditions, the annealing in a vacuum is used for preventing oxidation of the $Si_{0.7}Ge_{0.3}$ layer due to oxygen and water vapour diffusion into the second insulating layer 3 (SiO_2) deposited thereon, and the annealing in an N_2 atmosphere is used for causing selective oxidation of the conductive layer($Si_{0.7}Ge_{0.3}$) by means of the small amount of residual oxygen and water vapour that is present in the tube furnace diffusing into the second insulating layer (SiO_2), thereby to obtain effects of size and distribution changes of the quantum dots by germanium pileup and a germanium concentration change in the $Si_{0.7}Ge_{0.3}$ of the quantum dots.

The result of annealing under the atmospheric pressure of a tube furnace in an N_2 atmosphere is as follows. Figs. 4(a) and (b) illustrate cross-sectional TEM micrographs of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed in an N_2 atmosphere for 10 min. at 800 °C and 900 °C respectively. It can be seen from Fig. 4a that spherical quantum dots with a diameter of about 4.9×10^{-7} cm (49 Å) are formed. Considering the size and distribution of the quantum dots formed, it can be determined that the volume of the entire quantum dots has been

substantially reduced compared to the entire volume before the annealing, which may be on account of partial oxidation by the residual oxygen in the furnace. This can be proved indirectly by the fact that there are more quantum dots formed in the case of annealing in vacuum . It can be seen from Fig. 4b that the $Si_{0.7}Ge_{0.3}$ layer between the SiO_2 layers has disappeared. It is considered that the oxygen and water vapour present in the furnace are diffused into the layer during the annealing and oxidize the $Si_{0.7}Ge_{0.3}$ layer as the annealing proceeds under the atmospheric pressure of the tube furnace. Hardly any difference of agglomeration with respect to the annealing time period can be found, seemingly due to a very fast agglomeration time period. Accordingly, annealing for 1 hour and for 10 minutes show identical results. Fig. 5 illustrates a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}G_{0.3}/SiO_2$ structure annealed in an N_2 atmosphere for 10 min at 800 ^{0}C, from which it can be determined that the quantum dots formed have an average diameter of $4.9x10^{-7}$ cm (49 Å) with an r.m.s of $1.26x10^{-7}$ cm (12.6 Å) and a substantially uniform spatial distribution. The size and spatial distribution of the quantum dots are shown in Figs. 6a and 6b.

An $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed for 10 min. at 800 ^{0}C in a vacuum, excluding any influence from ambient, is compared with the above case when the structure is annealed in an N_2 atmosphere, from which it is found that the quantum dots obtained by annealing in vacuum have an average diameter of $3.6x10^{-7}$ cm (36 Å) with an r.m.s of $1.33x10^{-7}$ cm (13.3 Å), smaller than the case of annealing in an N_2 atmosphere. Fig. 7 is a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed at 800 ^{0}C for 10 min. in vacuum. Quantum dots annealed for 1 hour and for 10 minutes respectively show

no difference in average sizes. Fig. 8 is a plan-view of a TEM micrograph of an $SiO_2/Si_{0.7}Ge_{0.3}/SiO_2$ structure annealed at 800°C for 1 hour in vacuum, Fig. 9a illustrates a quantum dot size distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800 °C for 10 min. in vacuum, and Fig. 9b illustrates a spatial quantum dot distribution of an $Si_{0.7}Ge_{0.3}$ sample annealed at 800 °C for 10 min. in vacuum. It can be determined from Fig. 9b that the average concentration of the quantum dots annealed in vacuum, being $146/(0.1\mu m)^2$, is about 4 times higher than the average concentration of the quantum dots annealed in an N_2 atmosphere under the atmospheric pressure in the tube furnace, being $38/(0.1\mu m)^2$. This result indicates that there was selective oxidation of silicon by external oxygen or water vapour during annealing in the case of annealing under an N_2 atmosphere, resulting in consumption of the silicon, whilst there was no consumption of silicon by external oxygen or water vapour in the case of annealing under vacuum.

The described method of forming quantum dots has the following advantages.

Firstly, by means of the interface agglomeration, uniform sized $Si_{0.7}Ge_{0.3}$ quantum dots of a 3~4 nm range with uniform spatial distributions of $9.07/(0.1\mu m)^2$(annealing under vacuum) and $3.56/(0.1\mu m)^2$(annealing under an N_2 atmosphere) in r.m.s. can be obtained.

Secondly, annealing under vacuum allows the formation of quantum dots having a concentration higher than those annealed under an N_2 atmosphere in the atmospheric pressure in a tube furnace[$146/(0.1\mu m)^2$ under vacuum vs. $38/(0.1\mu m)^2$ under an N_2 atmosphere], with a smaller average size 3.6×10^{-7}cms (36Å) under vacuum vs. 4.9×10^{-7} cms (49Å) under an N_2 atmosphere). By changing the annealing atmosphere, the size and distribution

of the quantum dots can be controlled utilizing selective oxidation of silicon in $S_{1-x}Ge_x(0<x<1)$.

Thirdly, being a method for forming quantum dots suitable for application in an SET or an optical device such as a light emitting device, the interface agglomeration allows the formation of very small and uniform quantum dots compared to other existing methods, such as EBL, RIE and chemical synthesizing.

Claims:

1. A method of forming quantum dots in a semiconductor device, comprising the steps of:

forming an insulating layer on a substrate;
forming a conductive layer on the insulating layer;and,
annealing the conductive layer on the insulating layer to agglomerate the conductive layer.

2. A method as claimed in claim 1, wherein the insulating layer comprises a silicon oxide film.

3. A method as claimed in claim 1 or Claim 2, wherein the conductive layer comprises an alloy(Si_{1-x}-$metal_x$) of Si and a material selected from Si, Ge, $Si_{1-x}Ge_x$, Al, Au, Cu, Pt, Cr, Ru and Ta, or an alloy(Ge_{1-x}-$metal_x$) of Ge and said material, or an alloy($metal_{1-x}$-$metal_x$) of said materials, where $0<x< 1$.

4. A method of forming quantum dots in a semiconductor device, comprising the steps of:

forming a first insulating layer on a substrate;
forming a conductive layer on the first insulating layer;
forming a second insulating layer on the conductive layer; and,
annealing the conductive layer between the first and second insulating layers to agglomerate the conductive layer.

5. A method as claimed in claim 4, wherein each of the first and second insulating layers comprises a silicon oxide film.

6. A method as claimed in claim 4 or claim 5, wherein the conductive layer comprises an alloy($Si_{1-x}metal_x$) of Si and a material selected from Si, Ge, Si_{1-x} Al, Au, Cu, Pt, Cr, Ru and Ta, or an alloy(Ge_{1-x}-$metal_x$) of Ge and said material, or an alloy($metal_{1-x}$-$metal_x$) of said materials, where $0<x<1$.

7. A method as claimed in any one of claims 4 to6, wherein the first insulating layer comprises a thermal oxidation film, and the second insulating layer comprises a CVD oxidation film.

8. A method as claimed in any one of claims 4 to 7, wherein each of the first and second insulating layers comprises a silicon oxide film, and the conductive layer comprises $Si_{0.7}Ge_{0.3}$.

9. A method as claimed in any one of claims 4 to 8, wherein the first insulating layer is formed to a thickness of $4.4x10^{-6}$ to $5.5x10^{-6}$ cms (440 ~550 Å), the conductive layer is formed to a thickness of $3.0x10^{-7}$ to $5.0x10^{-7}$ cms (20~50 Å), and the

second insulating layer is formed to a thickness of $1.0x10^{-6}$ to $1.5x10^{-6}$ cm(100~150 Å).

10. A method as claimed in any one of claims 4 to 9, wherein the first insulating layer is deposited with SiO_2 to a thickness of $4.4x10^{-6}$ to $5.5x10^{-6}$ cms (440~550 Å) at 400~550 °C by LPCVD, the conductive layer is deposited with $Si_{0.7}Ge_{0.3}$ to a thickness of $3.0x10^{-7}$ to $5.0x10^{-7}$ cms (20~50 Å) at 300~450 °C, and the second insulating layer is deposited with CVD-SiO_2 to a thickness of $1.0x10^{-6}$ to $1.5x10^{-6}$ cm (100~150 Å) at 300~450 °C.

11. A method as claimed in any one of the preceding claims, wherein the annealing is conducted in a vacuum.

12. A method as claimed in any one of claims 1 to 10, wherein the annealing is conducted in an atmosphere of nitrogen.

13. A method of forming quantum dots in a semiconductor device, substantially as hereinbefore described with reference to the accompanying drawings.

14. A semiconductor device having quantum dots formed therein in accordance with any one of the preceeding claims.

15. A semiconductor device having quantum dots formed therein, substantially as hereinbefore described with reference to the accompanying drawings.

The Patent Office

21

INVESTOR IN PEOPLE

Application No: GB 9824541.8
Claims searched: all

Examiner: Martyn Dixon
Date of search: 18 February 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K (KEAX,KELX,KFX,KHAC,KKAX,KKB,KLHA,KLHX,KLX, KMWP,KMWX)

Int Cl (Ed.6): H01L; H01S

Other: Online: EPODOC,WPI,JAPIO,INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	US 5559343 A (Fujitsu) see e.g. col 3, lines 10-21 and col 4, line 44 to col 5, line 59	1,4
X,P	Journal of Crystal Growth, vol 192, no 3-4, pp 395-401, 1 Sept 1998, "Fabrication of nano-crystal silicon on SiO_2 using the agglomeration process", Sugiyama *et al*, see abstract	1,2,11
X,P	Japanese Journal Of Applied Physics, Part 2 (Letters), vol 37, no 2A, ppL161-L163, 1 Feb 1998, "Formation of nanostructures by oxidation of Si at low temperatures", Kyoung Hwan Koo *et al*, see abstract	1,2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.